

REMARKS

Upon entry of the present amendment, claims 1-16 will have been amended for consideration by the Examiner.

In view of the herein contained amendments and remarks, Applicants respectfully request reconsideration and withdrawal of each of the outstanding rejections set forth in the above-mentioned Official Action, together with an indication of the allowability of all of the claims pending in the present application.

Applicants initially note with appreciation the Examiner's indication that claims 2-8 and 10-16 would be allowable if rewritten in independent form.

Applicants further note with appreciation the Examiner's consideration of the documents cited in the Information Disclosure Statement filed November 19, 2001, by the return of the initialed and signed copy of the PTO-1449 Form accompanying the Information Disclosure Statement.

Applicants further respectfully request the Examiner's consideration of the documents cited in the Information Disclosure Statement filed May 28, 2004, by return of a initialed and signed copy of the PTO-1449 Form accompanying the Information Disclosure Statement filed therein. Applicants note that this IDS was filed after the mailing of the present Official Action.

Applicants further note with appreciation the Examiner's acknowledgment of Applicants' claim for foreign priority under 35 U.S.C. § 119 and receipt of the certified copy of the priority document.

Finally, Applicants note with appreciation the Examiner's acceptance of the drawings filed October 18, 2004.

In the Official Action, the Examiner has objected to claim 2 for having a double recitation. In response thereto, Applicants have amended claim 2 to clarify that the same circuit is being referenced. Applicants respectfully assert that the objection to claim 2 has been overcome.

In the Official Action, the Examiner has rejected claims 1 and 9 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,144,412 to HIRANO et al. in view of U.S. Patent No. 5,315,327 to SUZUKI.

Applicants respectfully traverse and assert that the rejection is inappropriate based on the remarks contained herein.

The present disclosed invention is directed to a video signal conversion device that converts an input video signal to a video signal suitable for a matrix display type device. As disclosed, an input video signal is input once in a storage, so as to carry out vertical frequency conversion, interlace-to-progressive conversion, scanning line number conversion, and horizontal pixel number conversion by using data stored in the storage.

As indicated by the Examiner in the Official Action, HIRANO et al. does not disclose a vertical frequency conversion processor. On the contrary, HIRANO et al. discloses an image processing device that converts a picture signal of interlaced scanning into that of progressive scanning by interpolation processing (See column 6, lines 29-38).

The HIRANO et al. device then performs horizontal scaling processing for expansion and compression and subsequent vertical scaling processing (See column 6, lines 53-60).

Further contrary to the present invention, the HIRANO et al. device merely inputs the picture signal without converting the vertical frequency to the IP converter. The input picture signal is stored once in a field memory for delay when subjected to interpolation processing in the IP converter in order to produce an interpolation signal. HIRANO et al. does not disclose the features of the present invention, including, inter alia, a storage, a vertical frequency conversion processor, an interlace-to progressive conversion processor, a scanning line conversion processor, a horizontal pixel conversion processor, and a synchronous controller, wherein the input video signal is stored once in the storage to carry out vertical frequency conversion, interlace-to-progressive conversion, scanning line number conversion, and horizontal pixel number conversion by use of data stored in the storage part.

More specifically, HIRANO et al. fails to disclose a storage part that stores the input video signal, and a vertical frequency conversion processor that outputs a write control signal for writing the video signal in the storage and a read control signal for reading the video signal stored in the storage to control input/output of the video signal in/from said storage part while converting the vertical frequency of the video signal by use of data stored in said storage part as recited by claim 1.

The Examiner relies on SUZUKI to show a vertical frequency converter. In this regard, SUZUKI discloses a memory controller 5 that includes a write control on the

basis of at least a horizontal scanning frequency. However, the SUZUKI controller does not convert a vertical frequency while outputting a write control signal and read control signal. More specifically, SUZUKI merely discloses an apparatus that converts a high speed television signal to a reference television signal by expanding the time axis of the high speed television signal by using odd and even field memories in which data write control and data read control are carried out by a memory controller.

Thus, SUZUKI also fails to disclose the features of the present disclosed invention, including, inter alia, a storage part, a vertical frequency conversion processing circuit, an interlace-to-progressive conversion processing circuit, a scanning line conversion processing circuit, a horizontal pixel conversion processing circuit and synchronous control circuit, wherein the input video signal is once stored in the storage part to carry out vertical frequency conversion, interlace-to-progressive conversion, scanning line number conversion and horizontal pixel number conversion by use of data stored in the storage part.

Moreover, SUZUKI also fails to disclose a storage that stores the input video signal, and a vertical frequency conversion processor that outputs a write control signal for writing the video signal in the storage part and a read control signal for reading the video signal stored in the storage part to control input/output of the video signal in/from said storage part while converting the vertical frequency of the video signal by use of data stored in said storage part as recited by claim 1; and SUZUKI also fails to disclose outputting a write control signal for writing the input video signal in the storage and a

read control signal for reading the video signal stored in the storage and for controlling input/output of the video signal in/from the storage while converting the vertical frequency of the video signal by use of data stored in the storage as recited by claim 9.

According to the present disclosed invention, the vertical frequency of a video signal stored in the storage part is converted. When this vertical frequency-converted video signal is an interlace signal, the video signal is converted from the interlace signal to a progressive signal. Then, the number of scanning lines of the interlace-to-progressive-converted video signal is converted, and the number of horizontal pixels of the scanning line-converted video signal is converted. The video signal is stored once in the storage, so that by using data stored in the storage, processing of vertical frequency conversion, IP conversion, scanning line conversion and horizontal pixel conversion are carried out. This enables provision of a system in which the four processes that are necessary for a matrix display device are integrated. This integrated system provides a much more simple configuration than the systems in which those processes are carried out by individual circuits.

Moreover, the horizontal pixel conversion processor is arranged at a succeeding stage, so that a lower sampling frequency is set in advance in analog to digital conversion to reduce the amount of data to be stored in the storage. Finally, the horizontal pixel conversion processing is carried out horizontal enlargement processing. This allows the above-described process to be carried out by use of a much smaller amount of data.

Moreover, there is no suggestion or disclosure in HIRANO et al. or SUZUKI separately or in any proper combination that render obvious the features of the present claimed invention including, inter alia, converting a vertical frequency while outputting a write control signal and read control signal as set forth in both independent claims 1 and

9. Accordingly, the Examiner is respectfully requested to withdraw the rejection under 35 U.S.C. § 103.

Additionally, minor amendments have been made to claims 1-15 in order to improve the language thereof. In these amendments, Applicants have made several changes to the language of the claims to render the same more self consistent, as well as more fully in compliance with U.S. syntax, idiom and grammar. These amendments do not change the scope of the claims but are merely cosmetic changes that give rise to no file wrapper estoppel.

In view of the fact that none of the art of record, whether considered alone or in any proper combination, discloses or suggests the present invention as defined by the pending claims, and in further view of the above remarks, reconsideration of the Examiner's action and allowance of the present application are respectfully requested and are believed to be appropriate.

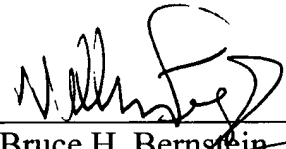
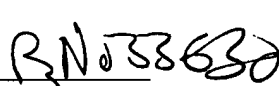
SUMMARY AND CONCLUSION

Applicants have made a sincere effort to place the present application in condition for allowance and believe that they have now done so.

Any amendments to the claims which have been made in this amendment, and which have not been specifically noted to overcome a rejection based upon the prior art, should be considered to have been made for a purpose unrelated to patentability, and no estoppel should be deemed to attach thereto.

Should the Examiner have any questions or comments regarding this Amendment, or the present application, the Examiner is invited to contact the undersigned at the below-listed telephone number.

Respectfully submitted,
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